REMARKS

This is in response to the Office Communication mailed on December 1, 2004, and a telephone call from the Examiner received on January 26, 2005. The Communication stated that the previously submitted Amendment failed to comply with 37 CFR §41.202(a)-(6) in that it failed to specifically apply each limitation or element of each copied claim to the disclosure to the application. The earlier version of this response provided this information. In the telephone call, the Examiner indicated that, more properly, 37 CFR §41.202(a)(1)-(6), needed to be complied with. Consequently, this information is being presented at this time in the following pages.

As noted, the previously submitted Amendment substituted new claims 19-24 for the previously pending claims. These newly added claims are directed to a coarse-fine programming method. Claims 19-24 are respectively exact copies of claims 1-6 of U.S. patent number 6,621,742, of Yamada, issued September 16, 2003.

Consequently, in response to the various portions of 37 CFR §41.202(a):

(1) Identification of Patent

Claims 19-24 are respectively exact copies of claims 1-6 of U.S. patent number 6,621,742, of Yamada, issued September 16, 2003.

(2) Identification of Claims Believed to Interfere, ProposedCount, and Claim Correspondence

Claims 19-24 are respectively exact copies of claims 1-6 of U.S. patent number 6,621,742, and, consequently, so correspond.

Claim 19 of the present application, which is an exact copy of claim 1 of U.S. patent number 6,621,742, is suggested as Count 1:

Count 1

> A method for programming a voltage threshold (Vt) level of a core cell in a memory device, the method comprising steps of:
>
> determining a desired Vt for the core cell;
>
> programming a portion of the Vt of the core cell using a selected programming strength;
>
> verifying that the portion of the Vt is successfully programmed;
>
> adjusting the selected programming strength; and
>
> repeating the step of programming, verifying, and adjusting until the Vt of the core cell is substantially equal to the desired Vt.

As claim 19 of the present application is a direct copy of the proposed Count 1, it so corresponds.

(3) Claim Chart for Count 1

As the proposed Count 1 is both Claim 19 of the present application and an exact copy of claim 1 of U.S. patent number 6,621,742, they correspond exactly:

Claim 19 of Present Application	Count 1
A method for programming a voltage threshold (Vt) level of a core cell in a memory device, the method comprising steps of: determining a desired Vt for the core cell;	A method for programming a voltage threshold (Vt) level of a core cell in a memory device, the method comprising steps of: determining a desired Vt for the core cell;
programming a portion of the Vt of the core cell using a selected programming strength;	programming a portion of the Vt of the core cell using a selected programming strength;
verifying that the portion of the Vt is successfully programmed;	verifying that the portion of the Vt is successfully programmed;
adjusting the selected programming strength; and	adjusting the selected programming strength; and
repeating the step of programming, verifying, and adjusting until the Vt of the core cell is substantially equal to the desired Vt.	repeating the step of programming, verifying, and adjusting until the Vt of the core cell is substantially equal to the desired Vt.

Claim 1 of U.S. patent number 6,621,742	Count 1
A method for programming a voltage threshold (Vt) level of a core cell in a memory device, the method	A method for programming a voltage threshold (Vt) level of a core cell in a memory device, the method

comprising steps of: determining a desired Vt for the core cell;	comprising steps of: determining a desired Vt for the core cell;
programming a portion of the Vt of the core cell using a selected programming strength;	programming a portion of the Vt of the core cell using a selected programming strength;
verifying that the portion of the Vt is successfully programmed;	verifying that the portion of the Vt is successfully programmed;
adjusting the selected programming strength; and	adjusting the selected programming strength; and
repeating the step of programming, verifying, and adjusting until the Vt of the core cell is substantially equal to the desired Vt.	repeating the step of programming, verifying, and adjusting until the Vt of the core cell is substantially equal to the desired Vt.

As the claims are identical and the present application will prevail on priority, as described in the next section, the claims interfere within the meaning of Sec. 41.203(a).

(4) How Applicant Will prevail on Priority

The present application is a continuation of U.S. patent application serial number 09/793,370 filed on February 26, 2001, and consequently is entitled to a priority date of February 26, 2001.

U.S. patent number 6,621,742 has a filing date of April 29, 2002, over a year after the priority date to which the present application is entitled.

(5,6) Claim Charts

The following claim charts are as previously submitted. They show the corresponding written description for each claim in the specification of the present application. They also show where the disclosure provides a constructive reduction to practice within the scope of the interfering subject matter.

Support for Claims

The material to which the pending claims are drawn is described most succinctly in the present application with respect to Figure 9 and its corresponding description, beginning on line 32 of page 16, although additional detail is found throughout the application. More specifically:

19. A method for programming a voltage threshold (Vt) level of a core cell in a memory device, the method comprising steps of:	The method is generally presented in Figure 9 for an exemplary emdobiment.
determining a desired Vt for the core cell;	Step 414, "Latch target data $D(S_i)$", where $D(S_i)$ corresponds to the desired Vt.
programming a portion of the Vt of the core cell using a selected programming strength;	Steps 430-438, particularly step 438, where the selected programming strength is $V_{STG}(i)$, selected in step 432..
verifying that the portion of the Vt is successfully programmed;	Step 436. The "portion of the Vt" is "target state S*i* within a Margin(Phase)".
adjusting the selected programming strength; and	Step 432 (in next phase after loop back from 460 to 420).
repeating the step of programming, verifying, and adjusting until the Vt of the core cell is substantially equal to the desired Vt.	The loop of steps 420-460, particular 438, 436, and 432 within each loop.
20. The method of claim 19, further comprising, after the step of verifying, a step of returning to the step of programming using the selected programming strength if it is determined that the portion of the Vt was unsuccessfully programmed.	The "No" path from 436 to 438, with the loop of steps 438 and 436 comprising a pulse-verify process.

21. The method of claim 20, wherein the step of adjusting is a step of weakening the selected programming strength.	Adjusting the Waveform according to the phase in Step 432. See also, for example, page 17, lines 1-3, or page 7, lines 24-26: "A second feature is to iterate the programming through a series of operation phases, where with each phase the programming waveform produces increasing finer programming steps."
22. The method of claim 20, wherein the step of adjusting is a step of weakening the selected programming strength as the Vt of the core cell approaches the desired Vt.	See 21. On "as Vt ... approaches the desired Vt", the second phase follows the first phase (Step 422).
23. The method of claim 20, wherein the step of adjusting is a step of weakening the selected programming strength after each successful step of verifying.	The successful verifying is the "Yes" path out of step 450, which leads to step 460 and the loop back to Step 420.
24. The method of claim 20, wherein the step of adjusting comprises steps of:	
using the same selected programming strength for a first selected number of programming steps; and	Description of step 450, page 18, lines 22-24: "If programming has passed a predetermined maximum allowed number of pulses ...".
weakening the programming strength for a second selected number of programming steps.	Step 450 is repeated in the loop of each phase.

As presented above, it is respectfully submitted that the present application supports all of the currently pending claims and an early indication of their allowability is earnestly solicited. In the meantime, a phone call to the undersigned is invited should there be any questions.

Respectfully submitted,

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